

A Pipelined Charge Division ADC Architecture for Low Power, HS Data Conversion

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An analog to digital conversion strategy that improves the -power product for GPS ADCs by more than an order of magnitude over existing devices is proposed. The architecture uses only 10 comparators for 10 bits of resolution (with no OpAmps), and produces a -bit digital output every clock cycle. It uses a -like approach, but the SAR approach has been modified to enable the ADC to accept a new analog input every clock cycle (i.e. it is a kind of pipelined SAR converter that functions using charge sharing).